

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO. LTD.,)	
SAMSUNG ELECTRONICS AMERICA, INC.,)	
SAMSUNG TELECOMMUNICATIONS)	
AMERICA GENERAL, LLC,)	
SAMSUNG SEMICONDUCTOR, INC., and)	
SAMSUNG AUSTIN SEMICONDUCTOR LLC,)	
)	C.A. No. 06-720 (***)
Plaintiffs,)	
)	REDACTED
v.)	PUBLIC VERSION
)	
ON SEMICONDUCTOR CORP. and)	
SEMICONDUCTOR COMPONENTS)	
INDUSTRIES, LLC,)	
)	
Defendants.)	

DECLARATION OF BRADLEY J. BOTSCH
IN SUPPORT OF MOTION TO DISMISS

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Original Filing Date: December 27, 2006
Redacted Filing Date: January 8, 2007

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I, Bradley J. Botsch, declare:

1. I am the Vice President and Chief Intellectual Property Officer of Semiconductor Components Industries, LLC, (hereafter "ON Semiconductor"). The following declaration is based on my personal knowledge. If called upon to testify, I could testify competently as to the matters set forth herein.

2. On September 15, 2005, I sent a letter to Mr. Jay Shim, who is Vice President, General Manager, and General Patent Counsel at Samsung Electronics Co. Ltd. ("Samsung"). I sent this letter to initiate negotiations for a potential license of U.S. Patent Nos. 5,563,594 ("the '594 Patent") and 6,362,644 ("the '644 Patent"). A true and correct copy of the letter is attached as Ex. 1.

3. Following this initial letter, Samsung and ON Semiconductor engaged in negotiations regarding a potential license of the '594 and '644 patents to Samsung. The negotiations later expanded to include U.S. Patent No. 5,361,001 ("the '001 Patent"). The negotiations included in-person meetings and telephone calls.

4. On December 1, 2005, ON Semiconductor and Samsung met in San Francisco, California. Jeong Woo Lee, a Samsung manager, and Patrick Muir, Samsung's outside counsel, were present and represented Samsung. Andy Williams, who at that time was ON Semiconductor's Vice President and General Manager; Paul Polansky, ON Semiconductor's outside licensing counsel; and myself were present and represented ON Semiconductor. No other people were present.

5. At this meeting the parties discussed a potential license of the '594 and '644 Patents. ON Semiconductor presented some slides, true and correct copies of which are attached as Exs. 2 and 3. Both parties presented different suggested constructions and analysis of relevant claims, and considered the other's proposals. ON Semiconductor also proposed that a license agreement could involve a cross-license with Samsung patents, although specific license

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proposals were not discussed. I did not mention litigation at this meeting, nor did I hear anyone else discussing litigation.

6. On February 15, 2006, ON Semiconductor and Samsung met in Dallas, Texas to further discuss a potential licensing agreement of the '594 and '644 Patents. Mr. Muir, Mr. Lee, and Andrew Hong, in-house counsel at Samsung, were present and represented Samsung. Mr. Polansky and myself were present and represented ON Semiconductor. No other people were present.

7. At this meeting, Samsung presented some slides, true and correct copies of which are attached as Exs. 4 and 5. Again, both parties presented different suggested constructions and analysis of relevant claims, and considered the other's proposals. I have reviewed the Declaration of Patrick Muir in which he asserts that I stated at this meeting that ON Semiconductor "would select their litigation targets carefully." I was present throughout the entire meeting and this statement was not made by me or anyone else. In fact, I did not mention litigation at this meeting, nor did I hear anyone else discussing litigation.

8. On April 24, 2006, I sent a letter by email to Samsung through Mr. Muir in order to initiate negotiations for a potential license of the '001 Patent. A true and correct copy of that letter with its enclosures is attached as Ex. 6.

9. Mr. Muir responded by email the same day. A true and correct copy of Mr. Muir's response is attached as Ex. 7.

10. Discussions between Samsung and ON Semiconductor regarding these patents as well as other ON Semiconductor patents that Samsung was interested in purchasing from ON Semiconductor continued through the end of July.

11. ON Semiconductor and Samsung met in person for a third time on August 16, 2006 for continued discussions directed to the potential license for ON Semiconductor's '594, '644, and '001 patents. Mr. Muir, Mr. Shim, and Bryan Richardson, Samsung's Intellectual Property Counsel, were present and represented Samsung. Peter Green, ON Semiconductor's

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Senior Vice President and General Manager, and I were present and represented ON Semiconductor. No other people were present.

12. At this meeting, ON Semiconductor made the first specific proposal for a license of the '594, '644, '001 patents, as discussed in a slide presentation. True and correct copies of the slides ON Semiconductor presented at that meeting are attached as Ex. 8. We proposed a

[REDACTED]
[REDACTED]
[REDACTED] As often happens with first offers in negotiations, Samsung said that it did not find this offer acceptable. Samsung, however, did not make a counteroffer or say what it would consider acceptable. ON Semiconductor stated that it still wanted to negotiate a resolution to this matter and did not want to litigate, but that ON Semiconductor did not intend to abandon its patent rights.

13. On September 6, 2006, I sent a letter by facsimile to Samsung, through Mr. Shim, following up on our August meeting. A true and correct copy of this facsimile is attached herewith as Ex. 9.

14. On September 15, 2006, I called Mr. Muir to ensure that Samsung had received my September 6, 2006 letter. Mr. Muir said that he had received the letter, but had not yet spoken to Mr. Shim. I advised that ON Semiconductor wanted to set up another meeting, and offered to meet with Samsung in Korea during the third week of November. I understand that Mr. Muir has alleged that during this call I said that ON Semiconductor was "considering filing a federal court litigation or ITC proceeding against Samsung." I did not make any such statement, and did not even mention litigation.

15. As a result of the September 15, 2006 call, the parties had a fourth in-person meeting to discuss the potential license agreement on September 29, 2006 in Korea. Mr. Shim, Mr. Lee, and one other local Korean Samsung employee were present and represented Samsung. I was present and represented ON Semiconductor. No other people were present.

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16. Mr. Shim advised on behalf of Samsung at the September 29, 2006 meeting that “I want to give value to your patents.” Mr. Shim stated that Samsung, however, would prefer [REDACTED]

[REDACTED]

[REDACTED] I responded that [REDACTED] could be acceptable to ON Semiconductor, but that we needed to hear a specific number from Samsung. Mr. Shim responded that he was “not prepared to do that today.” We ended the meeting by agreeing to meet again in November, each with concrete terms of proposed agreements. I reiterated to Samsung that, because ON Semiconductor had made the only offer to date, we wanted to hear a specific counteroffer from Samsung.

17. On Tuesday, October 31, 2006, Mr. Muir advised me by email that Samsung could participate in a meeting in Dallas on November 28, 2006. After I confirmed that Mr. Shim would be present, I agreed to the meeting. Attached as Ex. 10 is a true and correct copy of an email chain discussing this matter.

18. On Tuesday, November 21, 2006, while Mr. Shim was still in Korea, I called and emailed Mr. Shim to discuss ON Semiconductor’s concern about the value of traveling to Texas for a meeting if Samsung still was not prepared to respond to ON Semiconductor’s August 16, 2006 offer with its own counteroffer. A true and correct copy of the email I sent to Mr. Shim is attached as Ex. 11.

19. Mr. Shim did not return my call or email. I made repeated attempts to convey my message to Mr. Shim through emails and phone conversations to Mr. Shim and Mr. Muir. True and correct copies of email chains documenting some of these attempts are attached as Exs. 12 and 13.

20. Mr. Shim finally called me on November 27, 2006 around 6:00 p.m. local Arizona time to ask if we would be meeting the following day. I do not believe anyone else was involved in this telephone call. During the call, I reiterated that I did not see the worth of an in-person meeting unless Samsung was prepared to address ON Semiconductor’s initial offer with a

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counteroffer. Mr. Shim and I decided instead to schedule a telephone meeting at the time the in-person meeting would have been, at 1 p.m. local Arizona time on Tuesday, November 28, 2006.

21. On the next day, Tuesday, November 28, 2006, around 2 p.m. local Arizona time, I received a telephone call from Mr. Shim. I asked him to call me back at the telephone number of G. Sonny Cave, ON Semiconductor's Senior Vice President, General Counsel, and Chief Compliance and Ethics Officer, so that I could introduce Mr. Cave to Mr. Shim and so that Mr. Cave could participate in our negotiations. Mr. Shim responded, "I'm alone." When I stated that ON Semiconductor did not mind that Mr. Shim was alone, he agreed to call me back at Mr. Cave's telephone number.

22. Shortly thereafter, Mr. Shim called Mr. Cave's telephone line. I believe that only Mr. Shim, Mr. Cave, and I were involved in this telephone meeting. During this meeting, Mr. Shim stated twice that Samsung did "not want to litigate." Mr. Cave and I assured Mr. Shim that ON Semiconductor also preferred not to litigate the matter, and was seeking a business agreement. Mr. Cave then made an alternative proposal on behalf of ON Semiconductor for a license agreement. [REDACTED] Mr. Cave

proposed [REDACTED]
[REDACTED] Mr. Cave pointed out that this represented [REDACTED]

[REDACTED] Mr. Cave added that ON Semiconductor would entertain a counterproposal from Samsung [REDACTED]
[REDACTED]
[REDACTED]

23. Mr. Shim, who was in the United States at that time, responded that he would think about it and that he needed to talk to "my management and my board" in Korea to get "approval" and would call ON Semiconductor the next day around 5 or 6 p.m. Mr. Shim gave no indication that he found our offer unreasonable or too high, and I believed the fact that he said

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he was seeking board approval before responding indicated that Mr. Shim hoped to accept our offer or at least to finally make a counteroffer.

24. On Wednesday, November 29, 2006, around 5:30 p.m. local Arizona time, Mr. Shim called to advise me that he had not yet been able to contact the “right people” in Korea, but that he planned to do so that evening and would call me again the following day around the same time. Mr. Shim also inquired as to whether Mr. Cave and I would be available for a face-to-face meeting in Dallas on Friday. I answered that I was available and that I would check on Mr. Cave’s availability. I believe that Mr. Shim and I were the only people involved in this telephone call.

25. On Thursday, November 30, 2006, around 5:30 p.m. local Arizona time, Mr. Shim called me. I believe that Mr. Shim and I were the only people involved in this call. On this call Mr. Shim advised me for the first time that the parties were “very far apart,” and that as a result, Samsung had filed a declaratory judgment action against ON Semiconductor regarding the ‘594, ‘644, and ‘001 patents earlier in the day. Then, Mr. Shim told me that Samsung was withholding service of process because it “did not want to go down the litigation path” and hoped to settle the matter directly with ON Semiconductor. Finally, Mr. Shim made Samsung’s first specific offer to license the ‘594, ‘644, and ‘001 patents.

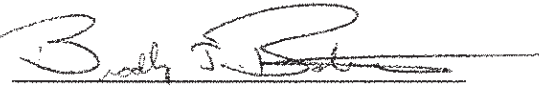
26. Samsung’s November 30, 2006 offer included [REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]

27. I never threatened Samsung with litigation regarding the ‘594, ‘644, and ‘001 Patents, nor did I witness anyone else representing ON Semiconductor making such statements.

28. I have reviewed the December 26, 2006 Declaration of G. Sonny Cave and concur in his description of the November 28, 2006 teleconference between myself, Mr. Cave, and Mr. Shim (¶¶ 4-6).

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I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

By: 
Bradley J. Botsch

549900

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CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on December 27, 2006, I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Josy W. Ingersoll
John W. Shaw

I also certify that copies were caused to be served on December 27, 2006, upon the following in the manner indicated:

BY HAND

Josy W. Ingersoll
John W. Shaw
YOUNG, CONAWAY, STARGATT & TAYLOR LLP
The Brandywine Building
1000 West Street, 17th Flr.
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BY FEDERAL EXPRESS

John M. Desmarais
James E. Marina
Kirkland & Ellis LLP
153 East 53rd Street
New York, NY 10022


/s/ Karen Jacobs Loudon

Karen Jacobs Loudon
klouden@mnat.com

CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on January 8, 2007, I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Josy W. Ingersoll
John W. Shaw

I also certify that copies were caused to be served on January 8, 2007 upon the following in the manner indicated:

BY HAND

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/s/ Karen Jacobs Louden (#2881)

Karen Jacobs Louden
klouden@mnat.com

EXHIBIT 1



ON Semiconductor
Law Dept., M/D A700
5005 East McDowell Road
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Brad.Botsch@onsemi.com
Direct Line: 602/244-5358
Facsimile: 602/244-5601

September 15, 2005

VIA FEDERAL EXPRESS and FACSIMILIE

Mr. Jay Shim, Esq.
Vice President, General Manager & General Patent Counsel
Samsung Electronics
445-701
San #16 Banwol-Ri, Taeon-Eup,
Hwasung-City, Gyeonggi-Do, KOREA
(82)-(31)-208-7398-7399 (FAX)

Re: Availability of License for Double Data Rate (DDR) DRAMs
from ON Semiconductor

Dear Jay:

I hope you are doing well. It has been a while since we have last met which I believe was in Korea last October. As I am sure you heard, I left AMD back in October of 2004 and I am now the General Patent Counsel of Semiconductor Components Industries LLC (d/b/a ON Semiconductor). As part of my activities at ON Semiconductor, I had the opportunity to review in detail its patent portfolio. Based on that review, I would like to direct your attention to U.S. Patent Nos. 5,563,594 ("the '594 patent") and 6,362,644 (the '644 Patent), both of which are owned by ON Semiconductor. A copy of these two patents are attached for your reference.

ON Semiconductor believes that all of Samsung's DDR and DDR-2 SDRAM memory devices infringe one or more claims of the '594 Patent. As an example,

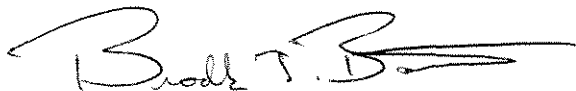
Mr. Jay Shim
September 15, 2005

Samsung's 512 MB DDR SDRAM device having part number K4H510838B infringes one or more claims of the '594 Patent. Further, ON Semiconductor also believes that all of Samsung's DDR-2 SDRAM memory devices infringe one or more claims of the '644 Patent. As an example, Samsung's 512 MB DDR-2 SDRAM device having part number K4T51163Q infringes one or more claims of the '644 Patent.

ON Semiconductor would be pleased to provide Samsung with a nonexclusive license under the '594 and '644 Patents. Accordingly, I will be contacting you in the near future to discuss potential dates for a meeting in Seoul or Hwasung in which we can discuss these patents in more detail as well as the details of a suitable licensing arrangement. In the mean time, please feel free to contact me at (602) 244-5358 if you have any questions.

Very truly yours,

SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.



Bradley J. Botsch
General Patent Counsel and Director of Intellectual Property

Enclosure: copy of U.S. Patent Nos. 5,563,594 and 6,362,644

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EXHIBIT 2

EXHIBIT 2 HAS BEEN REDACTED
IN ITS ENTIRETY

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EXHIBIT 3

EXHIBIT 3 HAS BEEN REDACTED
IN ITS ENTIRETY

PUBLIC VERSION - REDACTED

EXHIBIT 4

EXHIBIT 4 HAS BEEN REDACTED
IN ITS ENTIRETY

PUBLIC VERSION - REDACTED

EXHIBIT 5

EXHIBIT 5 HAS BEEN REDACTED
IN ITS ENTIRETY

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EXHIBIT 6

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**REDACTED AS
PRIVILEGED**

From: Bradley Botsch
Sent: Monday, April 24, 2006 9:53 AM
To: 'Patrick Muir'
Cc: 'jshim@samsung.com'; 'Paul J. Polansky'
Subject: ON Patent - Stolfa
Importance: High

Patrick

Please see the attached letter and the two supporting documents. Paul and I will be happy to discuss this at your earliest convenience.

Best Regards,

Bradley J. Botsch
Vice President and Chief Intellectual Property Officer
ON Semiconductor
5005 East McDowell Road, MD A700
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(602) 244-5358
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Samsung 042406 Letter.pdf



US5361001 (Stolfa).pdf



5361001 (Stolfa)_Samsung.pdf



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April 24, 2006

VIA FEDERAL EXPRESS and FACSIMILIE

Mr. Patrick D. Muir, Esq.
Muir Patent Consulting
758 Walker Road
Great Falls, VA 22066

Re: Additional ON Semiconductor Patent of Interest to Samsung

Dear Patrick:

It was good to speak to you last week about resolving our discussion, and we hope to reach an amicable resolution soon.

ON Semiconductor continues to review its patent portfolio with respect to Samsung products. We now want to direct your attention to U.S. Patent No. 5,361,001 ("the '001 patent"). A copy of this patent is attached for your reference.

ON Semiconductor believes that the '001 Patent is of interest to Samsung's gDDR3 SDRAM memory devices. As an example, ON Semiconductor believes that the '001 Patent is of interest to Samsung's 512 MB gDDR3 SDRAM having part number K4J52324QC-B. An exemplary claim chart is attached hereto.

Lets continue our discussions about a suitable licensing arrangement in the near future. I will give you a call soon to discuss next steps, but please feel free to contact me at (602) 244-5358 if you have any questions in the mean time.

Very truly yours,

SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.

A handwritten signature in dark ink, appearing to read "Brad J. Botsch", written over a horizontal line.

Bradley J. Botsch
Vice President and Chief Intellectual Property Officer

cc: Mr. Jay Shim, Esq., Samsung (no encl.)

encl.: U.S. Patent No. 5,361,001
Claim chart for the '001 Patent

US005361001A

United States Patent [19][11] **Patent Number:** **5,361,001****Stolfa**[45] **Date of Patent:** **Nov. 1, 1994**[54] **CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING**

0262716 10/1990 Japan 307/202.1

[75] Inventor: **David L. Stolfa**, Phoenix, Ariz.*Primary Examiner—Margaret Rose Wambach
Attorney, Agent, or Firm—Robert D. Atkins*[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.[21] Appl. No.: **160,762**[22] Filed: **Dec. 3, 1993**[51] Int. Cl.⁵ **H03K 3/01; H03B 1/04**[52] U.S. Cl. **327/530; 327/525; 327/312**

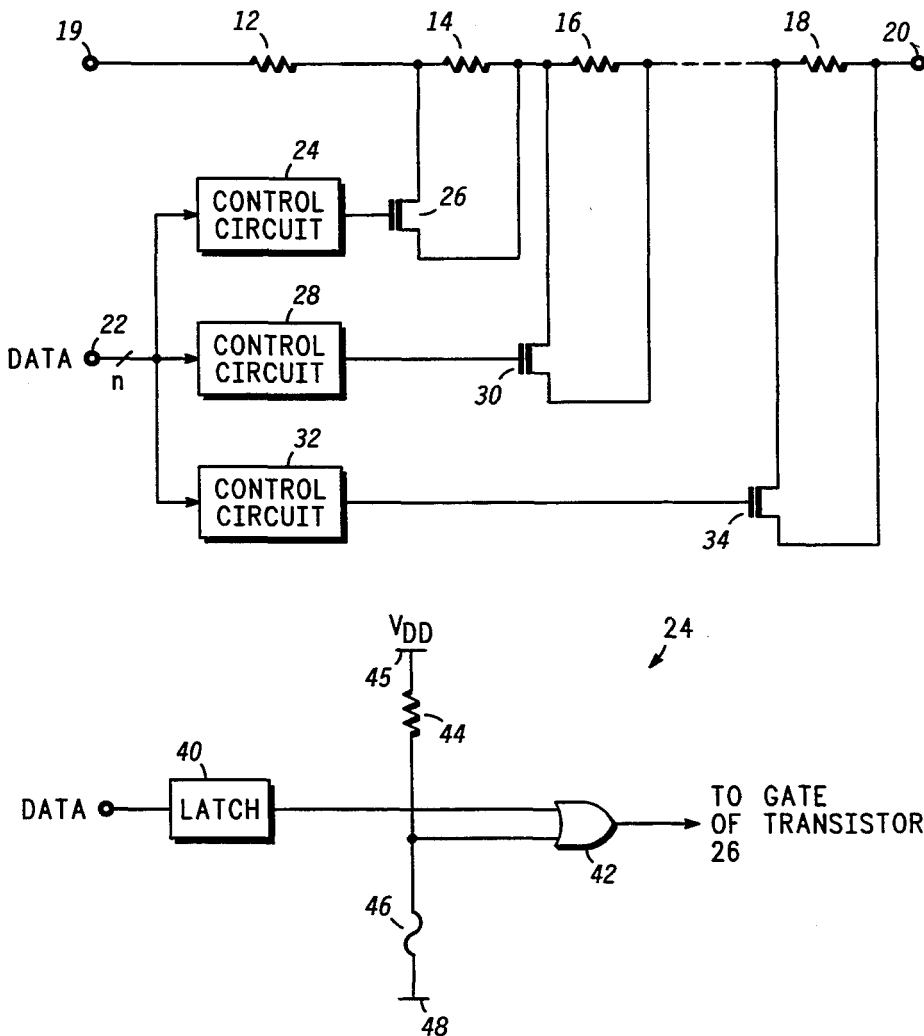
[58] Field of Search 307/202.1, 296.1, 547, 307/548

[56] **References Cited****U.S. PATENT DOCUMENTS**4,158,786 6/1979 Hirasawa 307/296.1
4,446,534 5/1984 Smith 307/202.1**FOREIGN PATENT DOCUMENTS**

0112298 5/1987 Japan 307/202.1

7 Claims, 1 Drawing Sheet[57] **ABSTRACT**

An analog trim circuit enables and disables one or more serially connected passive elements for setting characteristics of the circuit. Each passive element has a transistor across its first and second conduction terminals operating in response to a control signal from a control circuit for enabling and disabling conduction through the associated passive element. The control circuits are responsive to a data signal for providing the control signals that enable and disable the conduction through the passive elements. The data signal allows a preview of the trimming results. The fuse in certain ones of the control circuits are blown to set the control signals to fixed values after removal of the data signal.



U.S. Patent

Nov. 1, 1994

5,361,001

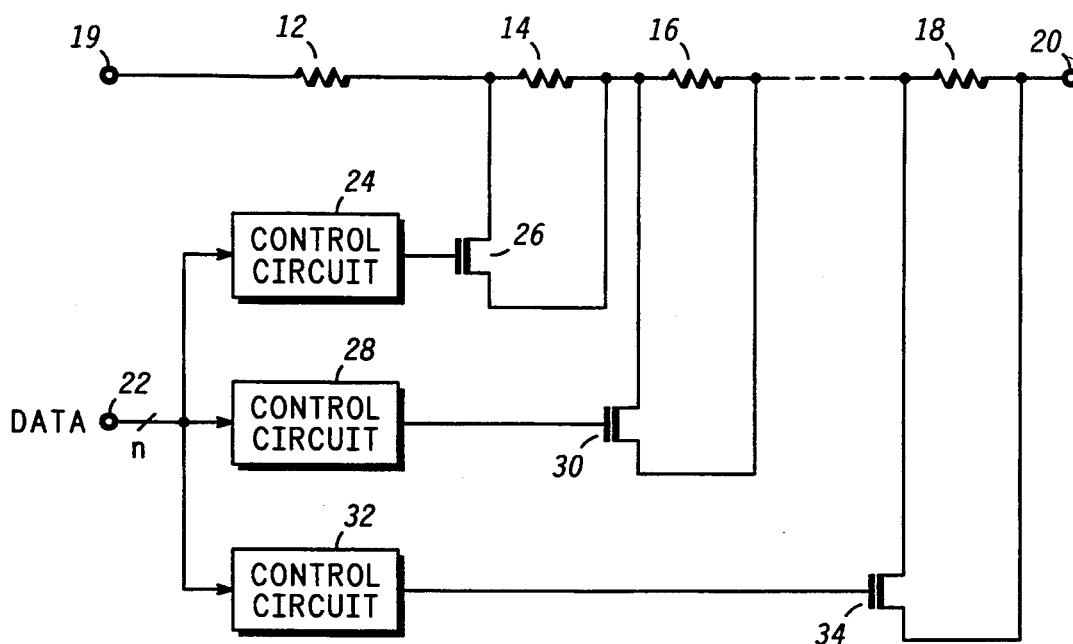
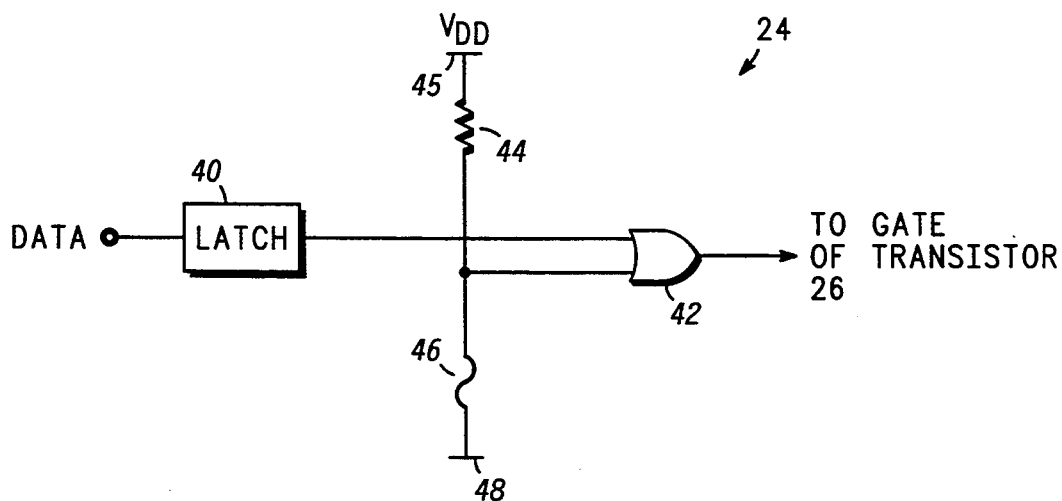


FIG. 1

↑
10

FIG. 2



5,361,001

1

CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING

BACKGROUND OF THE INVENTION

The present invention relates in general to analog trim circuits and, more particularly, to a technique of previewing the analog trim results before blowing a fuse to lock the trim in place.

In manufacturing analog integrated circuits, the basic building blocks are usually not accurately controlled by the manufacturing process as may be desired. For example, capacitors and resistors may have the wrong value, and MOS transistors may have the wrong gain setting. There are too many variables in the manufacturing process to yield absolute predictable results. Yet historically analog circuits often require very accurate voltage references, frequency references, and accurately ratioed elements.

To compensate for the process variability, many electronic circuits use analog trimming during test to set resistor values as necessary for proper operation of the circuit. A typical trimming technique utilizes a resistor ladder comprising a series of serially coupled resistors each in parallel with either a fuse or anti-fuse. A fuse is a device that is substantially an electrical short until it is blown open. An anti-fuse is an electrical open until blown when it becomes substantially an electrical short.

The fuse-blowing approach may take several forms, each with its own shortcomings. Laser fuses may be used directly across each resistor element in the ladder to enable and disable conduction through the resistor. During test, certain resistors are selected to open the shunt element thereby adding resistance to the serial path. The resistor ladder should be adjustable at wafer test over a range from say 10 to 2,560 ohms in 10 ohm increments.

The analog trimming may be performed iteratively, i.e. test, trim, test, trim, to measure the effect of the course trim and determine the necessary fine trimming. For iterative trimming, a laser trim system is typically installed on the wafer tester to alternately test and trim. However, one laser system per tester is very expensive. The laser is often in an idle state waiting for the tester. Moreover, if either the test system or laser breaks down both are inoperative.

An alternate approach is to use a zener anti-fuse across the resistor ladder. Such an element can be cheaply trimmed on the tester so that iterative testing can be done in one pass on the tester. Zener anti-fuses require large currents to program. Therefore, each anti-fuse requires its own external pad and probe card needle. This restricts the programming bit count to say 5-10 bits before the die area for test pads and complexity of the probe card requirements become prohibitive.

In general, iterative testing is a slow and expensive process. Consequently, many trimming techniques utilize only a single pass to evaluate which resistors in the serial string should be included to achieve the desired analog circuit operation. Thus, as result of a test measurement, the user blows the shunt fuse elements whereby the circuit is expected to operate as planned. The process of blowing the fuses typically involves laser trimming off-line from the test set to cut the poly material and open the shunt element. The circuit may be returned to the test set to verify proper trimming. If the subsequent testing should fail, the part is typically dis-

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carded since it is difficult to patch the shunt fuse elements.

Hence, a need exists for an iterative trimming to evaluate the results of test before permanently setting the trim.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram illustrating an analog trimming circuit; and

FIG. 2 is a schematic diagram illustrating the control circuit of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An analog trim circuit is shown in FIG. 1 including a passive ladder network 10 comprising resistors 12, 14, 16 and 18 serially coupled between terminal 19 and terminal 20. Resistor 12 is non-trimmable and provides the minimum ladder resistance (R_{MIN}). Resistors 14-18 are selected in an exponential series, such as 1280, 640, 320, 160, 80, 40, 20, and 10 ohms. Resistors 14-18 are passive elements each with first and second conduction terminals. Other passive elements may also be used in the trim circuit. A data signal is applied at terminal 22. One bit of the data signal is applied to each of control circuits 20, 28 and 32. An address signal selects the control circuit to latch one bit of the data signal.

Control circuit 24 provides a control signal to the gate of MOS transistor 26. The drain and source of transistor 26 are coupled to first and second conduction terminals of resistor 14. Likewise, control circuit 28 provides a control signal to the gate of MOS transistor 30 which has its drain and source coupled across resistor 16. Control circuit 32 provides a control signal to the gate of MOS transistor 34. The drain and source of transistor 34 are coupled across the first and second conduction terminals of resistor 18. The effective resistance through resistor ladder 10 is thus temporarily set by transistors 26, 30 and 34 selectively enabling and disabling conduction through resistors 14-18 upon receiving a high state or low state of control signals from control circuits 24, 28 and 32. With the above trimming scheme, the resistor ladder is controllable from R_{MIN} to $R_{MIN} + 2,560$ ohms assuming eight trimmable resistors in 256 possible 10 ohm increments.

Turning to FIG. 2, further detail of control circuit 24 is shown. Control circuits 28 and 32 follow a similar construction and operation as described for control circuit 24. The data signal is latched in latching circuit 40 for application to a first input of OR gate 42. An address signal enables latching circuit 40 to latch the data bit. Resistor 44 is coupled between the second input of OR gate 42 and power supply conductor 45. Power supply conductor 45 operates at a positive potential VDD such as 5 volts. Fuse 46 is coupled between the second input of OR gate 42 and power supply conductor 48 operating at ground potential. The output of OR gate 42 provides the control signal to the gate of transistor 26. An alternate embodiment of control circuit 24 may replace OR gate 42 with a NAND gate while resistor 44 and fuse 46 exchange places in the circuit.

Trim circuits are used in a variety of applications. For example, a circuit may require a given frequency f_0 determined by an RC time constant such that the frequency is inversely proportional to RC. The resistance R and capacitance C should be selected such that the nominal process target values of sheet ρ (resistance per

5,361,001

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unit area) and capacitance per unit area yield the desired frequency f_o . However, the actual process values of resistance and capacitance may vary by 5%-10%. Thus, the trimmable resistor ladder 10 must be trimmed to compensate for any variation in sheet ρ and capacitance per unit area.

During testing at wafer level, the circuit under test is exercised and any correction necessary to resistor ladder 10 is calculated by a binary search. Steps are taken to determine whether a resistor should be trimmed such that it is in the upper half or lower half of its trimmable range, i.e. determining if the most significant bit or largest resistor should be shorted or left to remain in resistor ladder 10. With resistor ladder 10 trimmed to its most significant bit the circuit under test is again tested and a correction is calculated to determine if it should be trimmed to the upper half or lower half of the remaining trimmable range. As a result, the next most significant resistor is shorted or allowed to remain. The process continues until all trimmable resistors have been checked.

Consider the trimming operation during test where a logic one data signal is stored in latching circuit 40 of each of control circuits 24, 28 and 32. The output of each OR gate 42 goes high and enables transistors 26, 30 and 34. Resistors 14-18 are substantially shorted, i.e. disabling the conduction path through resistors 14-18. The resistance of ladder 10 is equal to R_{MIN} .

To perform trim preview during test, the data signal to control circuit 24 is set to logic zero and stored in its latching circuit 40. At wafer test all fuses are yet unblown so that all fuse inputs to the OR-gates are low. The control signal at the output of OR-gate 42 goes low and turns off transistor 26 to enable the conduction through resistor 14. The resistance of ladder 10 increases to $R_{MIN} + R_{14}$, where R_{14} is the value of resistor 14. The effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. If more resistance is needed, the data signal to control circuit 28 may be set to logic zero. The control signal to transistor 30 goes low as described above for control circuit 24. Transistor 30 turns off and enables the conduction through resistor 16. The resistance of ladder 10 increases to $R_{MIN} + R_{14} + R_{16}$, where R_{16} is the value of resistor 16. Again, the effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. The process continues until the circuit under test operates as desired. Note at this point, the trimming process is temporary and dependent on the data signals to control circuits 24, 28 and 32. No fuses have yet been blown to lock in the trim. Thus, different combinations of resistors 14-18 may be previewed and checked to achieve optimal results.

An alternate trim approach could initially set the data signals to logic zero in control circuits 24, 28 and 32. The output of each OR gate 42 goes low and disables transistors 26, 30 and 34. The shunt elements 26, 30 and 34 are substantially opened, i.e. enabling conduction through resistors 14-18, thereby making ladder 10 resistance maximum. The testing preview involves setting the data signals to logic one and iteratively enabling transistors 26, 30 and 34 to disable conduction through resistors 14-18 and reduce resistance in ladder 10. The process continues until the circuit under test operates as desired. Again, the trimming process is temporary and dependent on the data signals to control circuits 24, 28 and 32. No fuses have yet been blown to lock in the

4

trim. Different combinations of resistors 14-18 may be tried and checked to achieve optimal results.

Another embodiment of the present invention is to configure the resistor ladder with the resistors in parallel and the control transistors in series with each resistor.

For the circuits under test that functionally pass, the bit pattern of trim is recorded in a file by wafer and die site. The file accompanies the wafer to a laser fuse system where the selected fuses 46 are blown. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore the permanent trim. The control signals from control circuits 24, 28 and 32 are thus set to a fixed value by blowing the selected fuses 46 in the control circuits after removal of the data signal at terminal 22.

The fuses are generally doped polycrystalline silicon films sometimes silicided polycrystalline silicon films in the range of 10 to 500 ohms. The polysilicon film is usually made in the shape of a polysilicon resistor with a width five to ten times its length. The ends of the fuses are connected by metal interconnects to the relevant circuitry. The fuse usually has most or all overlying oxide layers removed. With the use of on-die alignment marks the laser beam of approximately 1 μm -2 μm beam width is focused on the center of the fuse. The laser beam is a pulsed signal of such an energy that the polysilicon is vaporized and the fuse is severed and therefore permanently no longer conductive.

A key feature of the present invention is to preview trimming at wafer test to provide an economical means of iteratively trimming the resistive ladder using data provided by the tester. A data signal selectively trims the resistor ladder. The trimming is temporary and may be modified with different data signals to achieve optimal results. When the proper pattern of trim bits is determined for each individual circuit under test, that data is recorded and transferred off-line to the laser trimmer along with the wafer. The laser trim system blows the appropriate fuses for each circuit under test according to the pattern previously determined by testing various trimming options. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore sets the permanent trim. The preview trimming process allows optimization of the bit pattern for trimming before the actual laser trimming. Furthermore, the testing and the fusing systems may remain separate without requiring multiple passes through each.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention.

I claim:

1. An analog trim circuit, comprising:
a passive element having first and second conduction terminals;

first means coupled across said passive element and operating in response to a control signal for enabling and disabling conduction through said passive element, said first means includes a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said

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source being coupled to said second conduction terminal, said gate being coupled for receiving said control signal; and

second means responsive to a data signal for providing said control signal to said first means to enable and disable said conduction through said passive element, said second means setting said control signal to a fixed value after removal of said data signal.

2. The analog trim circuit of claim 1 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

3. The analog trim circuit of claim 2 wherein said second means includes:

a latching circuit having an input coupled for receiving said data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a second resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

4. A method of analog trimming, comprising the steps of:

enabling conduction through a passive element in response to a first state of a control signal;

disabling conduction through said passive element in response to a second state of said control signal;

activating said control signal in response to a data signal to enable and disable said conduction

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through said passive element, said activating step including the steps

(a) latching said data signal, and

(b) logically combining said data signal with a logic signal for providing said control signal; and setting said control signal to a fixed value after removal of said data signal.

5. The method of claim 4 wherein said setting step includes the steps of:

removing said data signal; and

blowing a fuse to set said control signal at said fixed value.

6. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said source being coupled to said second conduction terminal, said gate being coupled for receiving a control signal;

a latching circuit having an input coupled for receiving a data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a first resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

7. The analog trim circuit of claim 6 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

* * * * *

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DOCUMENT HAS BEEN
REDACTED IN ITS ENTIRETY

PUBLIC VERSION - REDACTED

EXHIBIT 7

PUBLIC VERSION - REDACTED

REDACTED AS
PRIVILEGED

From: Patrick Muir [mailto:patrick@muirpatentconsulting.com]
Sent: Monday, April 24, 2006 11:02 AM
To: Bradley Botsch
Cc: jshim@samsung.com; 'Paul J. Polansky'; jeongwoo.lee@samsung.com
Subject: RE: ON Patent - Stolfa

Thanks Brad. We'll take a look and get back to you.

Patrick

From: Bradley Botsch [mailto:Bradley.Botsch@onsemi.com]
Sent: Monday, April 24, 2006 12:53 PM
To: Patrick Muir
Cc: jshim@samsung.com; Paul J. Polansky
Subject: ON Patent - Stolfa
Importance: High

Patrick

Please see the attached letter and the two supporting documents. Paul and I will be happy to discuss this at your earliest convenience.

Best Regards,

Bradley J. Botsch
Vice President and Chief Intellectual Property Officer
ON Semiconductor
5005 East McDowell Road, MD A700
Phoenix, Arizona 85008
(602) 244-5358
(602) 244-5601 (Fax)

PUBLIC VERSION - REDACTED

(602) 703-5286 (Cell)

PUBLIC VERSION - REDACTED

EXHIBIT 8

EXHIBIT 8 HAS BEEN REDACTED
IN ITS ENTIRETY

PUBLIC VERSION - REDACTED

EXHIBIT 9

PUBLIC VERSION - REDACTED

MESSAGE CONFIRMATION

SEP-06-2006 04:56 PM WED

FAX NUMBER : 6022445601
NAME : ON SEMI LAW

NAME/NUMBER : 901182312087399
PAGE : 3
START TIME : SEP-06-2006 04:52PM WED
ELAPSED TIME : 04'10"
MODE : STD ECM
RESULTS : [O.K]



ON Semiconductor

FAX TRANSMITTAL FORM
FAX: (602) 244-5601

TO: Jay Shim
COMPANY: Samsung
FAX: 82-31-208-7399 PHONE: _____
NUMBER OF PAGES INCLUDING THIS COVER: 3 DATE: September 6, 2006
FROM: Bradley J. Botsch *JB*

Check appropriate POPI classification of information being sent:

☐ ON Semiconductor General Business Information
☐ ON Semiconductor Internal Use Only
☐ ON Semiconductor Confidential Proprietary
☐ Other (Non-ON Semiconductor Business)

COMMENTS: See attached

IF THERE ARE ANY PROBLEMS WITH THIS TRANSMISSION, PLEASE CALL: (602) 244-6648

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ON Semiconductor
Law Dept., M/D A700
5005 East McDowell Road
Phoenix, AZ 85008
Brad.Botsch@onsemi.com
Direct Line: 602/244-5358
Facsimile: 602/244-5601

VIA FACSIMILE AND EMAIL

September 6, 2006

Jay Shim
Vice President/General Manager and General Patent Counsel
445-701 San #16 Banwol-Dong, Hwasung-City,
Gyeonggi-Do, KOREA
Facsimile (82) (31) 208-7399

Re: Confidential Settlement Discussions for U.S. Patent #s 5,563,594 and 6,362,644

Dear Jay,

Thank you again for our meeting held on August 16th in New Jersey. Peter and I very much appreciated the opportunity to explain in person our proposed business resolution with respect to Samsung's use of ON Semiconductor's ("ON") patents in connection with the manufacture and sale of DDR and DDR2 SDRAM products. As we conveyed at the August 16th meeting, ON is very committed to its patent licensing program and is indeed quite serious about its patent assertions with respect to Samsung. To this end, ON has expended considerable time, money and other resources to conduct extensive evaluations of the merits of these specific patent assertions and present our findings to Samsung in an amicable and professional manner so that we could explore and discuss mutually agreeable ways to resolve the issues. Based upon these thorough evaluations and our mutual discussions, ON also developed and presented a reasonable, good faith offer for Samsung to acquire relevant rights to ON's patents by entering into an appropriate licensing transaction with ON. In this connection, we delivered an outline of our offer at the August 16th meeting and requested that Samsung carefully consider it and provide ON with a response.

PUBLIC VERSION - REDACTED

As of this date, ON has received neither a substantive response from Samsung nor any indication whether such a response will be forthcoming in the near future. Given this lack of communication, ON is certainly left wondering whether Samsung intends to ignore ON's proposal and abandon any further discussions to resolve the underlying patent issues. If this is indeed the case, then we must reemphasize to you that Samsung's decision will lead ON to pursue other paths to enforce its legal rights and remedies. While we prefer to follow the current path of professional and amicable negotiation with Samsung, please rest assured that ON views this matter with the utmost seriousness and is prepared to pursue it to a final conclusion one way or another. If Samsung intends to continue working together with ON to find a negotiated solution, then Samsung needs to provide an appropriate explanation and substantive response to ON's proposal. In this connection, ON suggests that the parties get together again very shortly to review this matter and determine which path to resolution will be followed going forward.

Accordingly, I request that you contact me by **September 14th** with proposed dates for a meeting in September. In that connection, the ON team, including our General Counsel, Sonny Cave, would be willing to meet you in Korea or, alternately, in the U.S. if you plan to be here during this time frame. Please understand that ON expects a timely response to this letter and that a continuing lack of response will not advance our mutual interests in achieving a negotiated resolution.

Very Truly Yours,



Bradley J. Botsch
Vice President and Chief Intellectual Property Officer

cc: Patrick Muir, Esq.
Sonny Cave, Esq.
Peter Green

PUBLIC VERSION - REDACTED

EXHIBIT 10

PUBLIC VERSION - REDACTED

**DUPLICATE MESSAGE
DELETED**

Message from "Patrick Muir" <patrick@muirpatentconsulting.com> on Tue, 21 Nov 2006 10:16:04 -----
----- 0700-

<Bradley Botsch" <Bradley.Botsch@onsemi.com" :**To**
November 28th meeting :**Subject**

Hi Brad

We have a conference room at the Prava Suites ("Forth Worth" conference room). The Prava Suites are located next door to the Galleria in Dallas. The address is 13402 Noel Road / Dallas TX 75234. Phone is 972 503 8700.

We suggest starting at 2:00 PM. Does this work for you?

Patrick

Message from "Patrick Muir" <patrick@muirpatentconsulting.com> on Thu, 2 Nov 2006 07:09:40 -----
----- 0700-

<Bradley Botsch" <Bradley.Botsch@onsemi.com" :**To**
<Becky Newnam" <Becky.Newnam@onsemi.com" :**cc**
Re: November 28th :**Subject**

Brad

I'll get back to you regarding location after all our travel details get sorted out.

Patrick

PUBLIC VERSION - REDACTED

On 11/1/06 5:48 PM, "Bradley Botsch" <Bradley.Botsch@onsemi.com> wrote:

> Patrick

>

> The ON team will be available to meet with you, Jay and Jeong Woo on the

> afternoon of Tuesday (11/28) in Dallas, as you proposed. I assume that

> we will be meeting in your hotel. Will it be at the Galleria again?

> Please provide the appropriate meeting location details. Thanks.

>

> Regards,

> Brad

>

> -----Original Message-----

> From: Patrick Muir [<mailto:patrick@muirpatentconsulting.com>]

> Sent: Wednesday, November 01, 2006 6:32 AM

> To: Bradley Botsch

> Subject: Re: November 28th

>

> Brad,

>

> Jay plans to attend the 28th meeting as well. I'll wait to hear back

> from

> you whether or not the afternoon of the 28th works for you and your

> team.

>

> Patrick

>

>

> On 10/31/06 2:19 PM, "Bradley Botsch" <Bradley.Botsch@onsemi.com> wrote:

>

>> Patrick

>>

>> Thanks - without Jay, I am not sure what we would accomplish? My

>> understanding was that we were aiming to settle this matter and Jay

>> told

>> me during the September 29th meeting in Korea that he wanted to do a

>> cash settlement.

>>

>> Brad

>>

>> -----Original Message-----

>> From: Patrick Muir [<mailto:patrick@muirpatentconsulting.com>]

>> Sent: Tuesday, October 31, 2006 10:16 AM

>> To: Bradley Botsch

>> Subject: Re: November 28th

>>

>> I'm double checking and will get back to you.

>>

>> Patrick

>>

>>

>> On 10/31/06 2:01 PM, "Bradley Botsch" <Bradley.Botsch@onsemi.com>

> wrote:

>>

>>> Hi Patrick

PUBLIC VERSION - REDACTED

>>>>
>>>> Thanks for the follow up. I will check to see if this date is
>> available
>>>> for the ON team. I assume that Jay will also be attending this
>> meeting?
>>>> Please confirm.
>>>>
>>>> Brad
>>>>
>>>> -----Original Message-----
>>>> From: Patrick Muir [<mailto:patrick@muirpatentconsulting.com>]
>>>> Sent: Tuesday, October 31, 2006 9:50 AM
>>>> To: Bradley Botsch
>>>> Subject: November 28th
>>>>
>>>> Hi Brad,
>>>>
>>>> How are you? I understand that when you met with Jay in Korea, a
>> follow
>>>> up
>>>> meeting was proposed. How about meeting the afternoon of November
>> 28th
>>>> in
>>>> Dallas? Both Jeong Woo and I will be in Dallas at that time. Does
>> this
>>>> work for you?
>>>>
>>>> Patrick
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DUPLICATE MESSAGE
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PUBLIC VERSION - REDACTED

EXHIBIT 11

PUBLIC VERSION - REDACTED

**DUPLICATE MESSAGE
DELETED**

Message from "Bradley Botsch" <Bradley.Botsch@onsemi.com> on Tue, 21 Nov 2006 17:41:59 -----
----- 0700-

<jshim@samsung.com> :**To**
<Patrick Muir" <patrick@muirpatentconsulting.com" :**cc**
RE: November 28th meeting :**Subject**

Jay

I would like to have a brief telephone call with you as soon as possible regarding the agenda for this meeting next Tuesday. I have also left a message with your assistant on Wednesday morning (Korean time). Could you please call me on my cell phone (the number is included below)? Thanks.

Best Regards,

Bradley J. Botsch
Vice President and Chief Intellectual Property Officer
ON Semiconductor
5005 East McDowell Road, MD A700
Phoenix, Arizona 85008

PUBLIC VERSION - REDACTED

EXHIBIT 12

PUBLIC VERSION - REDACTED

**DUPLICATE MESSAGE
DELETED**

----- Original Message -----

Sender : Bradley Botsch<Bradley.Botsch@onsemi.com>

Date : 2006-11-28 00:24

Title : Re: November 28th meeting

Jay, Patrick

Please let me know if Samsung intends to present their reasonable first. As I have said before, ON does not want to negotiate against itself.

Thanks.

Brad Botsch

-----Original Message-----

From: Patrick Muir <patrick@muirpatentconsulting.com>

To: Bradley Botsch

Sent: Mon Nov 27 08:11:12 2006

Subject: Re: November 28th meeting

Brad,

My understanding is that both parties agreed to make reasonable proposals at this next meeting. I have not heard anything from Samsung to indicate that it has moved away from this agenda. I'm not sure what more I can tell you. Please let me know whether or not you decide to cancel tomorrow's meeting.

Thanks.

Patrick

p.s. - regarding e-mails to Samsung, make sure they have a subject typed in or they will be bounced by Samsung's e-mail security. If you want, forward me the e-mail and I'll forward it to Jay.

On 11/26/06 3:45 PM, "Bradley Botsch" <Bradley.Botsch@onsemi.com> wrote:

Patrick

Thanks. I did send Jay an email at jshim@samsung.com but it came back undelivered. More importantly, I left him an urgent message with his assistant for him to call me on Wednesday but I have not heard from Jay yet.

Anyway, Sonny and I have not booked our flights yet for Dallas. Therefore, you or Jay need to let me know by Monday morning whether Samsung intends on making a reasonable, bona fide and good faith response to ON's initial offer that was presented in New Jersey so that we can quickly schedule a flight.

PUBLIC VERSION - REDACTED

I look forward to hearing from you. Thanks.

Brad Botsch

-----Original Message-----

From: Patrick Muir <patrick@muirpatentconsulting.com>

To: Bradley Botsch

Sent: Sun Nov 26 06:34:14 2006

Subject: Re: November 28th meeting

Brad

As you requested, I sent an e-mail to Jay that you did not want to have a meeting if Samsung was not going to make an offer first. Please let me know if there is anything else you want to convey. Again, I think and e-mail to Jay directly makes the most sense for these communications.

Patrick

On 11/22/06 4:40 PM, "Bradley Botsch" <Bradley.Botsch@onsemi.com> wrote:

Patrick

I have not heard from Jay yet so if you talk to him, please have him call me (602 703-5286) or at least relay the general message. Thanks.

Brad

From: Patrick Muir [<mailto:patrick@muirpatentconsulting.com>]

Sent: Tue 11/21/2006 10:16 AM

To: Bradley Botsch

Subject: November 28th meeting

Hi Brad

We have a conference room at the Prava Suites ("Forth Worth" conference room). The Prava Suites are located next door to the Galleria in Dallas. The address is 13402 Noel Road / Dallas TX 75234. Phone is 972 503 8700.

We suggest starting at 2:00 PM. Does this work for you?

Patrick

PUBLIC VERSION - REDACTED

Message from "Bradley Botsch" <Bradley.Botsch@onsemi.com> on Mon, 27 Nov 2006 08:24:19 -----
----- 0700-

<patrick@muirpatentconsulting.com>, <jshim@samsung.com> :**To**
Re: November 28th meeting :Subject

Jay, Patrick

Please let me know if Samsung intends to present their reasonable first. As I have said before, ON does not want to negotiate against itself.

Thanks.

Brad Botsch

-----Original Message-----

From: Patrick Muir <patrick@muirpatentconsulting.com>
To: Bradley Botsch
Sent: Mon Nov 27 08:11:12 2006
Subject: Re: November 28th meeting

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Thanks.

Patrick

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Patrick

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Anyway, Sonny and I have not booked our flights yet for Dallas. Therefore, you or Jay need to let me know by Monday morning whether Samsung intends on making a reasonable, bona fide and good faith response to ON's initial offer that was presented in New Jersey so that we can quickly schedule a flight.

PUBLIC VERSION - REDACTED

I look forward to hearing from you. Thanks.

Brad Botsch

-----Original Message-----

From: Patrick Muir <patrick@muirpatentconsulting.com>

To: Bradley Botsch

Sent: Sun Nov 26 06:34:14 2006

Subject: Re: November 28th meeting

Brad

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Patrick

On 11/22/06 4:40 PM, "Bradley Botsch" <Bradley.Botsch@onsemi.com> wrote:

Patrick

I have not heard from Jay yet so if you talk to him, please have him call me (602 703-5286) or at least relay the general message. Thanks.

Brad

From: Patrick Muir [<mailto:patrick@muirpatentconsulting.com>]

Sent: Tue 11/21/2006 10:16 AM

To: Bradley Botsch

Subject: November 28th meeting

Hi Brad

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We suggest starting at 2:00 PM. Does this work for you?

Patrick

PUBLIC VERSION - REDACTED

EXHIBIT 13

PUBLIC VERSION - REDACTED

REDACTED AS
PRIVILEGED

Message from "Bradley Botsch" <Bradley.Botsch@onsemi.com> on Mon, 27 Nov 2006 17:41:27 -----
----- 0700-

<jshim@samsung.com> :To
patrick@muirpatentconsulting.com>, □□□ <kosb@samsung.com>, □□□>
<jeongwoo.lee@samsung.com> :cc
RE: Re: November 28th meeting Subject
:t

Jay

Welcome to Dallas. As I have told Patrick, I will attend the meeting if Samsung intends on starting the meeting off by making a reasonable, bona fide and good faith response to ON's initial offer that was presented in New Jersey. Please let me know if these are your intentions so that I can quickly schedule a flight.

Brad

From: 심재이 [mailto:jshim@samsung.com]
Sent: Monday, November 27, 2006 5:31 PM
To: Bradley Botsch
Cc: patrick@muirpatentconsulting.com; 고승범; 이정우
Subject: Re: Re: November 28th meeting

Brad:

PUBLIC VERSION - REDACTED

I've just arrived in Dallas to meet with OnSemi tomorrow at your request. My belief is that you will make a reasonable offer for settlement, and, of course, I intend to do my best. If you wish to cancel the meeting you should let me know immediately.

Jay

**DUPLICATE MESSAGE
DELETED**